Performance Analysis of Packed U-cell Multilevel Topology with Various Multicarrier Sine PWM Schemes

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***Abstract*—Multilevel DC to AC conversion is an attractive solution for high/medium power applications with improved power quality as compared to the classic two-level solution. Avenues are being also sought for implementing multilevel inverters for low power applications. Overall component count in conventional topologies is very high especially for a large number of output levels for enhanced power quality. Thus, modifications are being carried out in conventional topologies so as to reduce overall component count. In this paper, three such modified topologies are analysed in order to understand the possible pros and cons. Comments are made based on important qualitative and quantitative features. Simulation results are presented wherever necessary.**

***Index Terms*—Classical topologies, multilevel inverter, pulse width modulation (PWM), reduced component count, total harmonic distortion (THD).**

I. Introduction

Multilevel voltage source inverters have emerged as an effective solution for high power DC to AC conversion applications [1]. A multilevel inverter (MLI) comprises of multiple input DC levels (obtained from DC sources and/or capacitors) and power semiconductor devices to synthesize a stepped waveform. Blocking voltage requirements for the power switches are lower as compared to the overall operating voltage level [2]. In addition, the multilevel waveform exhibits better harmonic profile as compared to the conventional two-level waveform. Some other important advantages of MLIs are: reduced d*v*/d*t* stress on the load and possibility of fault tolerant operation [3]. Recent trends indicate that MLIs can also be employed for low power applications [4].

Quality of the multilevel waveform is further enriched by increasing the number of levels. This, however, inadvertently leads to the requirement of a large number of power semiconductor devices (accompanied with respective gate driver circuits). Thus system complexity and cost increase and overall system reliability and efficiency worsen. For high resolution waveform (implying a much better power quality), practical considerations necessitate reduction in overall component count [5].

The so-called 'conventional (or classic)' multilevel topologies which have been extensively studied and are commercially available are: neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitors (FC) converters [1, 3, 5-7]. These topologies exhibit a significant increase in the number of power switches, number of switches conducting simultaneously and overall cost of the system with the increase in the number of output levels. Researchers, therefore, continue to focus on reducing the component count in multilevel topologies through modifications in the conventional topologies. These modifications can be primarily characterized as: use of asymmetric sources [13-15] topological changes [8-12]; and combination of topological changes and asymmetric source configurations [16-18].

In this paper, one example each from the aforesaid modification strategies are studied and important observations are derived regarding reduction in component count, possibility of power balancing and optimal switching of power devices. Accordingly, the modified topologies may or may be employed depending on the application requirements.

The paper is organized as follows. Section II of the paper presents a general introduction on improvement of power quality through multilevel waveforms. Example of employing asymmetric source configuration in the classic cascaded H-bridge topology is presented in Section III. In Section IV, a modified H-bridge topology with an auxiliary bidirectional switch is discussed. A modified topology based on the flying capacitor structure which also employs asymmetric source configuration is analysed in Section V. Concluding remarks and inferences are summarized in Section VI.

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II. POWER QUALITY IMPROVEMENT

Power quality is quantitatively judged through a factor called 'total harmonic distortion (THD)' and through the presence of lower order harmonics which directly affect the filter size. Based on the type of output waveform, inverters can be classified as: square wave, quasi square wave, PWM and multilevel inverters. Because of their poor quality, square wave and quasi square wave inverters are not used for medium/high power applications. These inverters require bulky filters since the lower order harmonics are prominently present. A PWM inverter is controlled so as to imitate a pure sine wave, thereby reducing the lower order harmonics, though the higher order harmonics become more prominent. A multilevel waveform further reduces the presence of both lower order and higher order harmonics (thereby reducing the overall THD). Waveforms shown in Fig.1 corroborate these observations.

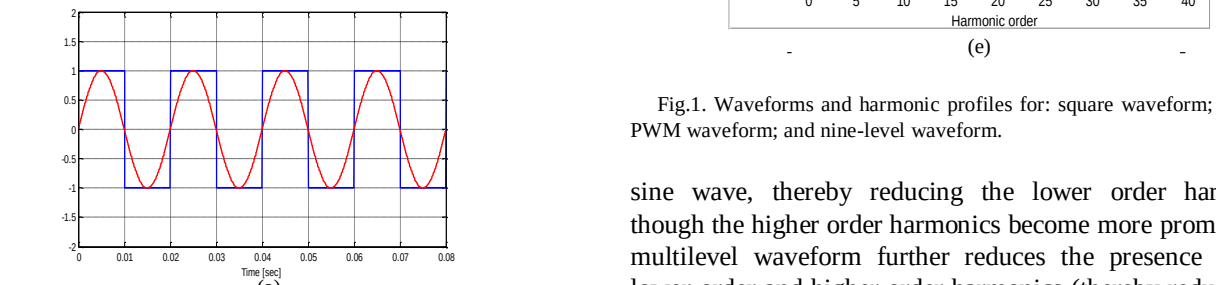

Fig.1. Waveforms and harmonic profiles for: square waveform; two-level PWM waveform; and nine-level waveform.

III. ASYMMETRY IN CLASSIC CHB TOPOLOGY

As shown in Fig.2, the cascaded H-bridge topology consists of series connected full bridges. In its classical form, the CHB consists of isolated DC sources with equal values (the configuration is referred to as 'symmetric source configuration'). In order to reduce the number of switches, researchers have proposed many 'asymmetric source configurations' where DC sources with unequal voltages are used [18]. The so-called 'binary' and 'trinary' configurations are very popular. A binary configuration, for example, utilizes eight number of power switches to synthesize seven levels while a trinary configuration synthesizes nine levels with eight switches. The classic structure would respectively require twelve and sixteen power switches for seven and nine level waveforms.

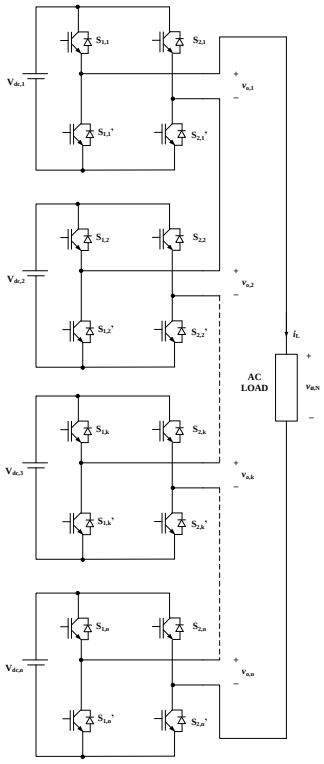

Fig.2. Cascaded H-Bridge topology

This reduction in number of switches has some important fallout. The asymmetric CHB structure becomes non-modular since differently rated switches are used. Modularity has been an important feature of the CHB topology. In addition, equal load sharing amongst the input DC sources cannot be programmed since the sources have different voltages and equal average currents cannot be derived without negatively affecting the output waveform.

IV. H-BRIDGE STRUCTURE WITH AUXILIARY BIDIRECTIONAL SWITCH

An interesting modification in the standard H-bridge structure is presented in [8] wherein an auxiliary bidirectional-conducting-bidirectional-blocking switch is added to increase the number of levels. The structure is shown in Fig.3.

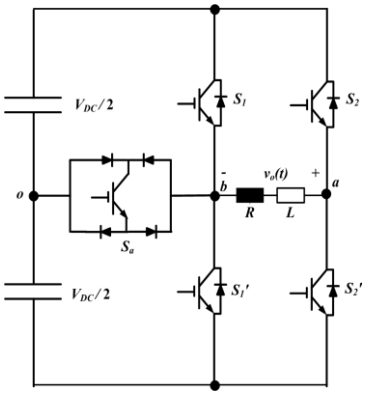

Fig.3. Modified H-bridge structure for a five-level output

While the standard H-bridge can synthesize two- or three-level waveform, the modified topology can synthesize five levels with the addition of just one switches. The classic CHB structure require eight switches for synthesizing five levels while the modified structure needs only five switches.

An important limitation of the modified topology is that it inadvertently requires a mix of unidirectional and bidirectional power switches, thereby posing design issues. In addition, the input DC sources mandatorily need to be symmetric. Also, no power balancing scheme can be implemented as the topology does not permit so.

VI. THE PACKED U-CELL TOPOLOGY

In [16], Youssef Ounejjar et al. have proposed a new power multilevel converter topology that is very competitive compared to the classical topologies. It consists of the so-called 'packed U cells'. Each U cell consists of an arrangement of two power switches and one DC input level (obtained with a voltage source or a floating capacitor). Authors claim that the topology offers high energy conversion quality using a small number of active and passive devices and consequently, has very low production cost. A single-phase structure of the packed U-cell topology with two input DC levels viz. $V_{DC,1}$ and $V_{DC,2}$, and six switches S_j {j = 1 to 6}, is shown in Fig.4.

The topology is very simple in terms of interconnection of components. The minimal voltage blocking capability required for switches (S_1 , S_2) is $V_{DC,1}$, while that for (S_5 , S_6) is $V_{DC,2}$. Voltage blocking capability for switches (S_3, S_4) is ($V_{DC,1}$ – $V_{DC,2}$). All the switches, when conducting, should be able to carry the load current. Various states for the structure are shown in Table I. Thus, to obtain a desired voltage level, only three switches conduct simultaneously. It is important to observe from Table I that to derive desired benefit from the topology, symmetric source configuration cannot be used as the output will be a three-level with many redundant states.

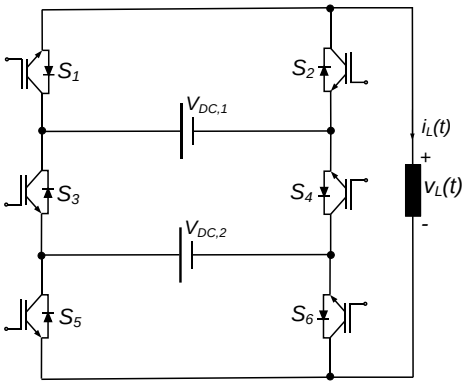

Fig. 4. Packed U-cell multilevel inverter topology as proposed in [16]

TABLE I
Switching states for topology shown in Fig.4

State	Output Voltage $v_L(t)$	Switches in ON state (other switches remain OFF)
1	0	S_1 , S_3 , S_5
2	0	S_2 , S_4 , S_6
3	$V_{DC,1}$	S_1 , S_4 , S_6
4	$V_{DC,2}$	S_1 , S_3 , S_6
5	$V_{DC,1} - V_{DC,2}$	S_1 , S_4 , S_5
6	$-V_{DC,1}$	S_2 , S_3 , S_5
7	$-V_{DC,2}$	S_2 , S_4 , S_5
8	$-V_{DC,1} + V_{DC,2}$	S_2 , S_3 , S_6

In fact, in [16], authors have proposed an elaborate methodology to calculate the asymmetric voltage levels. For two input levels, the number of output levels can be maximized with $V_{DC,1} = 3V_{DC}$ and $V_{DC,2} = V_{DC}$, however this trinary configuration synthesizes seven levels and not nine, because of the absence of additive combination. Thus for more number of input sources, trinary source configuration is not applicable. Hence, to derive optimal benefit from this topology, employing asymmetric source configuration is binding. For a structure with two input sources, switching of middle two switches viz. (S_3, S_4) can be performed at fundamental frequency as demonstrated in [16]. This feature, however, is not feasible for packed U cell based structures with more than two number of input DC levels. In [16], the authors implement source $V_{DC,2}$ with a floating capacitor in which the voltage is maintained at one-third of the voltage level $V_{DC,1}$. The control scheme, though, is fairly complex in nature.

VI. Conclusion

As multilevel inverters are gaining interest, efforts are being directed to reduce the device count for increased number of output levels. The merit of a multilevel inverter is enhanced by increasing the number of output levels but it inadvertently leads to increased number of components. Various approaches to reduce component count, taken by the researchers can be grouped as:

a. Topological modifications;
b. Employing asymmetric source configurations or asymmetric ratios of capacitor voltages; and
c. Combination of (a) and (b).

The attempt to reduce number of semiconductor switches in multilevel inverters involves one or more of the following compromises/challenges:

i. Increased power rating of semiconductor switches.
ii. Increased number of sources.
iii. Loss of modularity (as happens in asymmetric CHB topology).
iv. Reduced number of redundant states (as happens in asymmetric configurations).
v. Complex modulation / control schemes.
vi. Difficulty in possibility of charge balance control (especially in open loop mode).

Thus, implementing a modified topology would inculcate its own pros and cons and the application requirements would primarily govern the topology which has to be used.

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